BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP (303) 740-1980
Title: Reduced Hardware Network Adapter and Communication Method
Inventors: Michael R. Conley, et al.
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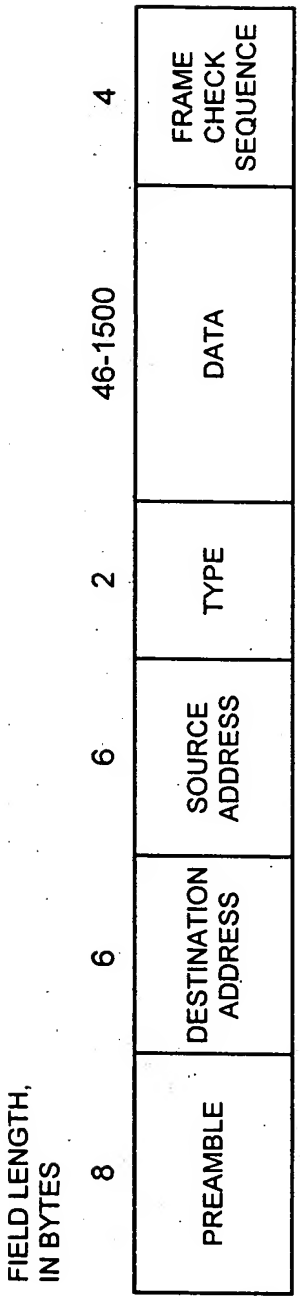


FIG. 1

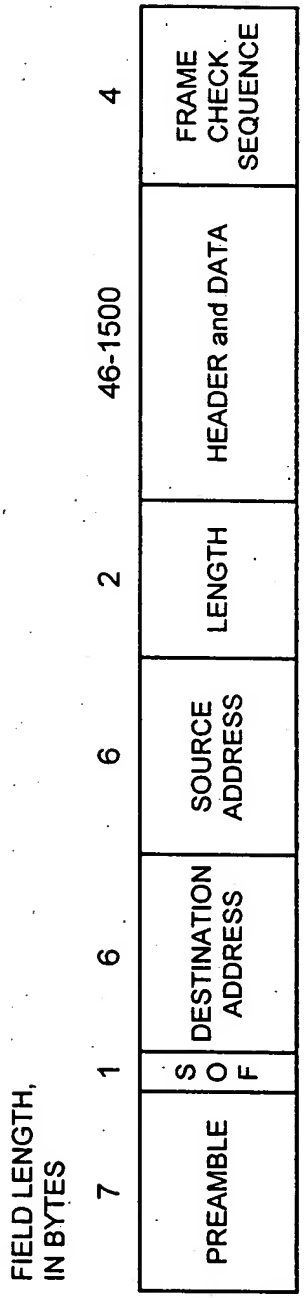


FIG. 2

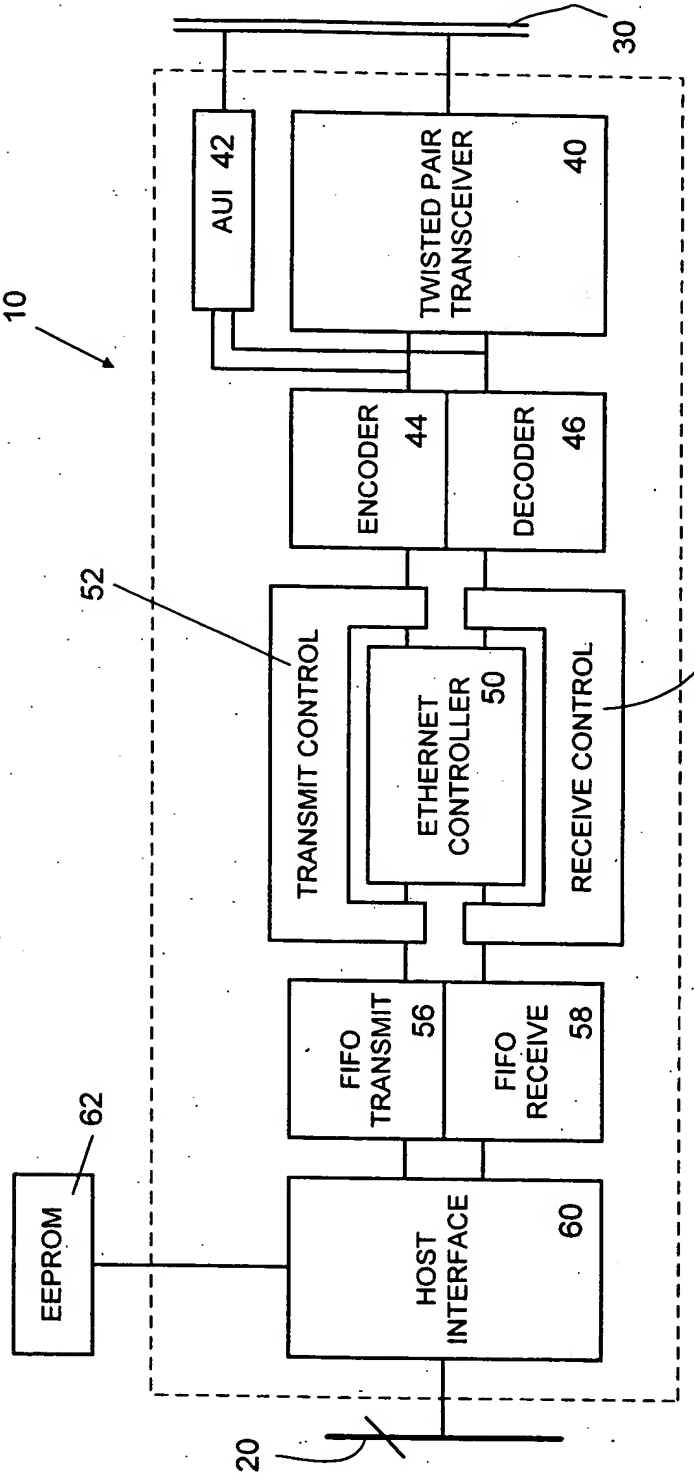
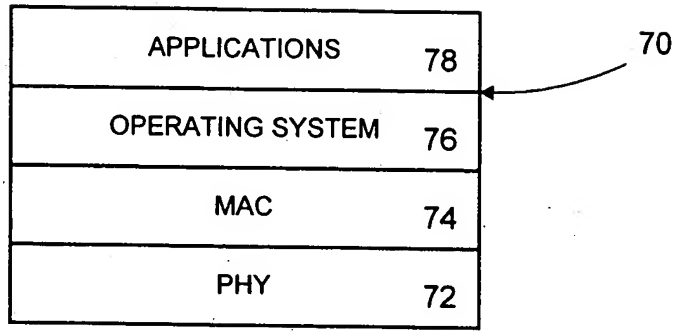

30
AUI 42
TWISTED PAIR TRANSCEIVER 40
10
ENCODER 44
DECODER 46
52
TRANSMIT CONTROL
ETHERNET CONTROLLER 50
RECEIVE CONTROL
54
FIFO TRANSMIT 56
FIFO RECEIVE 58
62
EEPROM
HOST INTERFACE 60
20

FIG. 3


APPLICATIONS
78
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OPERATING SYSTEM
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MAC
74
PHY
72

FIG. 4

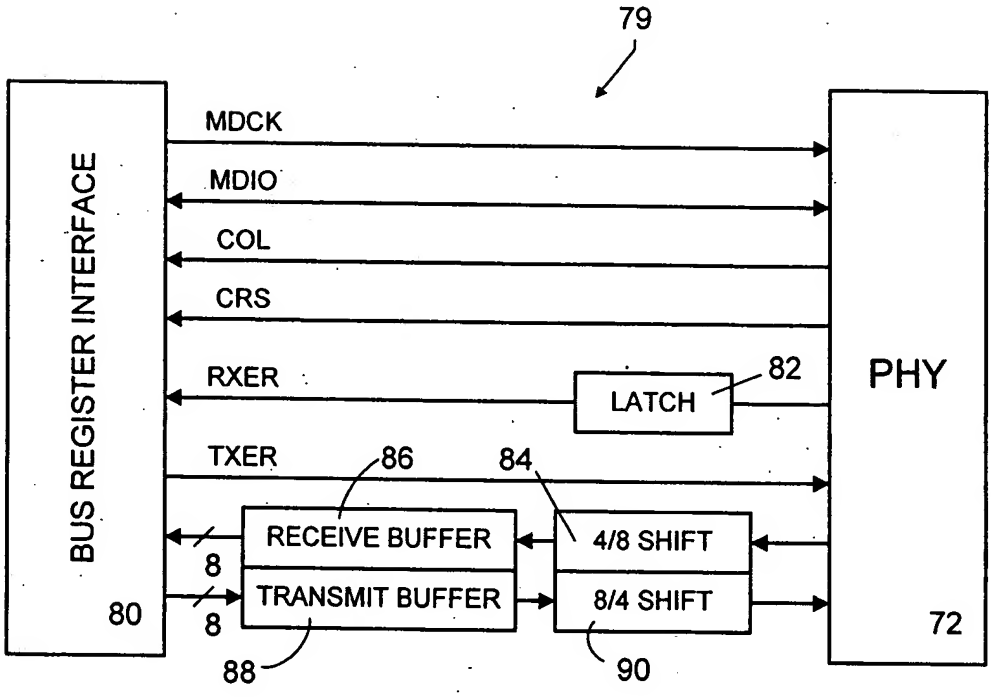
79
BUS REGISTER INTERFACE
80
MDCK
MDIO
COL
CRS
RXER
LATCH
82
PHY
TXER
86
84
RECEIVE BUFFER
4/8 SHIFT
8
TRANSMIT BUFFER
8/4 SHIFT
8
88
90
72

FIG. 5

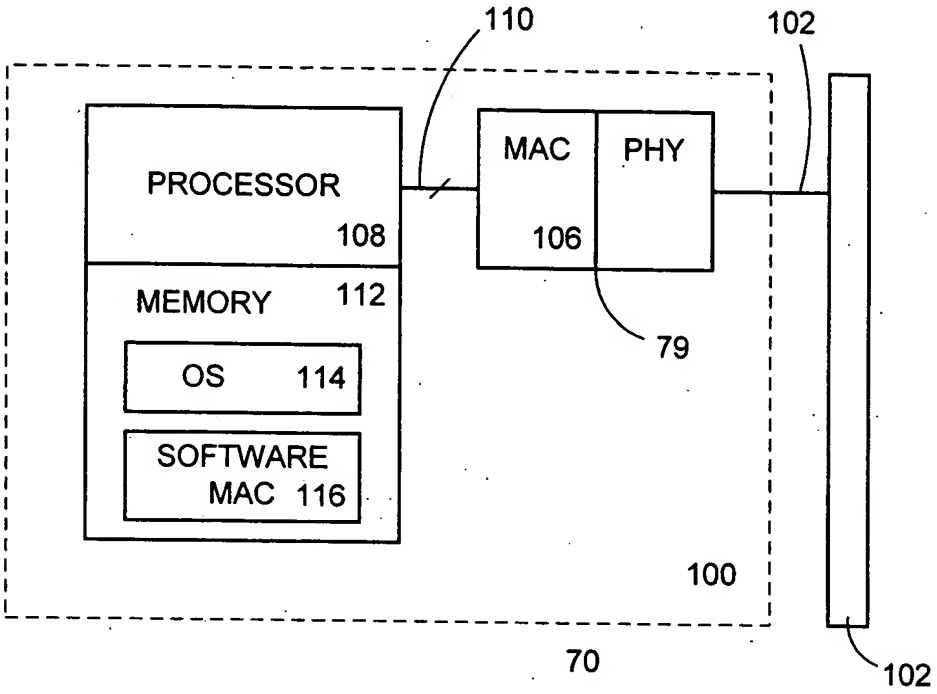

FIG. 6

ADDRESS	ABBREVIATION	NAME
0,1,2,3	ED	DATA REGISTER
4,5	BC	BYTE COUNT REGISTER
6	CS	COMMAND/STATUS REGISTER
7	MII	MII REGISTER

FIG. 7

DATA REGISTER					ADDRESS: 0,1,2,3			
BIT	7	6	5	4	3	2	1	0
DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0

FIELD	TYPE	DESCRIPTION
D[31:0]	R/W	THE DATA REGISTER IS THE INTERFACE TO THE RECEIVE AND TRANSMIT DATA BUFFER. READING FROM THIS REGISTER WILL RETRIEVE THE NEXT BYTES IN THE RECEIVE FIFO AND WRITING TO THIS REGISTER WILL PLACE THE DATA INTO THE TRANSMIT FIFO. ACCESSES CAN BE BYTE, WORD OR DWORD, BUT ACCESSES BEGIN AT ADDRESS 0.

FIG. 8

BYTE COUNT REGISTER					ADDRESS: 4,5			
BIT	7	6	5	4	3	2	1	0
DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0
BIT	15	14	13	12	11	10	9	8
DEFINITION	D15	D14	D13	D12	D11	D10	D9	D8

FIELD	TYPE	DESCRIPTION
D[15:0]	R/O	THIS IS A 16-BIT VALUE THAT REFLECTS HOW MUCH DATA IS CURRENTLY AVAILABLE IN THE RECEIVE FIFO. WHEN THIS REGISTER READS ZERO, THERE IS NO MORE DATA AVAILABLE.

FIG. 9

COMMAND/STATUS REGISTER					ADDRESS: 6 (WRITE)			
BIT	7	6	5	4	3	2	1	0
DEFINITION	RST							IE

FIELD	TYPE	DESCRIPTION
IE	W	SETTING THIS BIT ENABLES INTERRUPTS FROM THE ADAPTER
RST	W	SETTING THIS BIT RESETS THE ADAPTER. THIS BIT IS SELF CLEARING.

FIG. 10

COMMAND/STATUS REGISTER					ADDRESS: 6 (READ)			
BIT	7	6	5	4	3	2	1	0
DEFINITION					BC	COL	CRS	IP

FIELD	TYPE	DESCRIPTION
IP	R/O	INTERRUPT PENDING BIT (RESET ON A READ).
CRS	R/O	REAL-TIME CARRIER SENSE FROM THE PHY
COL	R/O	REAL-TIME COLLISION STATUS FROM THE PHY
BC	R/O	REAL-TIME DATA VALID FROM THE PHY

FIG. 11

MII REGISTER					ADDRESS: 7			
BIT	7	6	5	4	3	2	1	0
DEFINITION						MW	MC	MD

FIELD	TYPE	DESCRIPTION
MD	R/W	THIS BIT IS USED TO READ/WRITE DATA TO/FROM THE PHY MII. A READ OPERATION RETURNS THE CURRENT VALUE OF THE MDIO PIN ON THE PHY. THE MW BIT IS SET TO DRIVE THE MDIO PIN DURING A WRITE OPERATION.
MC	W	THIS BIT DRIVES THE MDCK PIN TO THE PHY, WHICH IS USED TO READ/WRITE TO/FROM THE PHY MII
MW	R/W	THIS BIT DETERMINES WHETHER THE MD BIT IS AN INPUT OR AN OUTPUT. SETTING THIS BIT WILL DRIVE THE VALUE OF THE MD BIT ON THE MDIO PIN TO THE PHY. THIS BIT SHOULD ONLY BE SET WHEN WRITING TO THE PHY MII.

FIG. 12